



Cap 2485 #3
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06-11-02

Dwyer 7-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s): Dwyer et al.
Case: 7-15
Serial No.: 09/975,762
Filing Date: October 9, 2001
Group: 2185
Examiner: Unassigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

Signature: Jim Thane Date: March 27, 2002

Title: Method and Apparatus for Reducing Cache Thrashing

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

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Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following document listed on the accompanying PTO Form 1449. A copy of the listed item is enclosed.

1. Kaxiras et al, "Cache Decay: Exploiting Generational Behavior to Reduce Cache Leakage Power," IEEE, (2001).
2. Lai et al., "Dead-Block Prediction & Dead-Block Correlating Prefetchers," IEEE, (2001).
3. Mendelson et al, "Modeling Live and Dead Lines in Cache Memory System," IEEE, Trans. on Computers, v. 42, no. 1, (January 1993).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,

Kevin M. Mason

Date: March 27, 2002

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FORM PTO-1449 (MODIFIED)

**LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT**



Applicant: Dwyer et al.
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U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
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FOREIGN PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES NO
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OTHER DOCUMENTS

EXAMINER	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Kaxiras et al, "Cache Decay: Exploiting Generational Behavior to Reduce Cache Leakage Power," IEEE, (2001).
		Lai et al., "Dead-Block Prediction & Dead-Block Correlating Prefetchers," IEEE, (2001).
		Mendelson et al, "Modeling Live and Dead Lines in Cache Memory System," IEEE, Trans. on Computers, v. 42, no. 1, (January 1993).

Examiner

Date Considered

1/7/04

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.